SYSTEM AND METHOD FOR POWER MANAGEMENT

TECHNICAL FIELD

[0001] Embodiments described herein generally relate to power management in a processor environment.

BACKGROUND

[0002] As electronic apparatuses become more complex and ubiquitous in the everyday lives of users, more and more diverse requirements are placed upon them. In addition, as capabilities of electronic apparatuses become more extensive, many users have become reliant on the enhanced performance such capabilities provide. As these aspects of electronic apparatuses have evolved, there has become an increasing need for reducing power consumption. However, under many circumstances, reducing power consumption may sacrifice performance. Therefore, it will be highly beneficial for a user to be able to have the desired performance when it matters the most to them, and optimize power performance during circumstances where performance may be less important to them. For example, many electronic apparatuses can operate in different power states (e.g., sleep states, idle states, etc.). In certain cases, unused resources can be turned off opportunistically. The significance of these activities can depend on the scope of resources available for minimizing power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Embodiments are illustrated by way of example and not by way of limitation in the FIGURES of the accompanying drawings, in which like references indicate similar elements and in which:

[0004] FIG. **1** is a flow diagram illustrating operations associated with power gating according to at least one example embodiment of the present disclosure;

[0005] FIG. **2** is a simplified table illustrating a comparison associated with at least one example embodiment of the present disclosure;

[0006] FIG. **3** is a block diagram illustrating components associated with determining latency tolerance according to at least one example embodiment;

[0007] FIG. **4** is a flow diagram illustrating runtime operations according to at least one example embodiment;

[0008] FIG. **5** is another flow diagram illustrating operations according to at least one example embodiment;

[0009] FIG. **6** is yet another flow diagram illustrating operations according to at least one example embodiment;

[0010] FIG. **7** is still another flow diagram illustrating operations according to at least one example embodiment;

[0011] FIG. **8** is yet still another flow diagram illustrating operations according to at least one example embodiment;

[0012] FIG. **9** is yet still another flow diagram illustrating operations according to at least one example embodiment;

[0013] FIG. **10** is yet still another flow diagram illustrating operations according to at least one example embodiment;

[0014] FIG. **11** is yet still another flow diagram illustrating operations according to at least one example embodiment;

[0015] FIG. **12** is yet still another flow diagram illustrating operations according to at least one example embodiment;

[0016] FIG. **13** is yet still another flow diagram illustrating operations according to at least one example embodiment;

[0017] FIG. **14** is a simplified block diagram associated with an example ARM ecosystem system on chip (SOC) of the present disclosure; and

[0018] FIG. **15** is a simplified block diagram illustrating example logic that may be used to execute activities associated with the present disclosure.

[0019] The FIGURES of the drawings are not necessarily drawn to scale or proportion, as their dimensions, arrangements, and specifications can be varied considerably without departing from the scope of the present disclosure.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0020] The following detailed description sets forth example embodiments of apparatuses, methods, and systems relating to providing a power savings in a processor environment. Features such as structure(s), function(s), and/or characteristic(s), for example, are described with reference to one embodiment as a matter of convenience; various embodiments may be implemented with any suitable one or more of the described features. It should be understood that terms such as "first", "second", etc. are merely used for differentiation purposes, and do not denote any sequential relationship, chronological relationship, and/or the like.

[0021] FIG. **1** is a block diagram illustrating components associated with providing power management according to at least one example embodiment. The examples of FIG. **1** are merely examples of components associated with providing power management, and do not limit the scope of the claims. For example, operations attributed to a component may vary, the number of components may vary, the composition of a component may vary, and/or the like. For example, in some example embodiments, operations attributable to one component of the example of FIG. **1** may be allocated to one or more other components.

[0022] In electronic devices, there is often a tradeoff between power saving and performance. Modern computer systems are typically formed of many semiconductor components that can communicate together via various interconnects such as those that are present on a circuit board. One common such interconnect mechanism (e.g., for incorporating various peripheral devices) is a Peripheral Component Interconnect Express (PCIe™) protocol in accordance with links based on the PCIe™ Specification (e.g., version 4.0, published on Nov. 29, 2011 (hereafter the PCIe™ Specification)). Note that the present disclosure is applicable to any version of the PCIe Specification. The interconnect can be formed of multiple layers, including a transaction layer, a link layer, and a physical layer (PHY). To reduce power consumption when communications are not occurring on a given interconnect, various mechanisms can be provided. If no communications are likely to occur for some time, the interconnect can be placed in a low-power state in which various interconnect circuitry can be disabled.

[0023] Typically, to determine when impending PCIe™ signaling is about to occur (e.g., when in an idle/sleep condition), squelching is a PCIe™ physical layer input/output (I/O) function to detect such signaling. Squelch logic attempts to detect voltage in receive pins of the interconnect to sense activity and prepare a link layer transaction state machine for proper operation to exit from the electrical state (EL) or lower power state. The squelch logic in the I/O circuit typically includes analog differential amplifiers, integrators, and other miscellaneous digital logic. The PHY